REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on February 7, 2007 and the references cited therewith.

Claims 1-23 are amended, no claims are canceled, and no claims are added; as a result, claims 1-23 are now pending in this application.

Objections to the Specification

The Office Action objected to the use of the phrase "can be associated" as it is used in describing spill instructions. The Office Action asserts:

> The specification mentions about an architecture having a set of primary and secondary registers as illustrated in Fig 2; and describes this using a phrase such as 'parallel register architecture'. For one skill in the art, the illustration of 2 rows of registers without further hardware specification in regard to a particular hardware-based architecture cannot achieve what is commonly accepted meaning for 'architecture' which entails much more hardware details. The Specification does not provide further details as how setting 2 registers in a Figure can make the registers an 'architecture' in the true meaning expected of it. It appears that the language used so to automatically raise the registers to the state of 'parallel register architecture' is inadequate if not improper, absent description needed to establish that the registers are only part of a more elaborate architecture, the architectural details about which apparently are not disclosed. The above phraseology will be treated as a setting wherein registers are disposed in columns or in plurality such that one set are more *primary* than another.[1]

Although Applicant does not agree with the assertions made in the Office Action, Applicant has amended the specification in order to facilitate prosecution. Applicant has replaced the words "primary" and "secondary" with "first" and "second", respectively. Applicant has also replaced the phrase "parallel register architecture" with "a CPU architecture having parallel registers." Support for this amendment can be found in the Instant Application *inter alia* at Page 8, Line 1.

Contrary to the Examiner's assertions, Applicant submits that the Specification does not indicate that the registers must be "disposed in columns." Despite the Examiner's assertions, Applicant submits that the Specification should be interpreted based on its language as understood by those of ordinary skill in the relevant art. The present amendments to the

[1] Office Action Page 2, Number 3

specification are only for facilitating expeditious prosecution of this application. Applicant believes the original language is clear and respectfully reserves the right to reintroduce the original language in a continuation application.

Claim Objections

The Office Action objected to claims 1, 9, 16, and 20. The Office Action asserted

> "the architecture limitation recited in the phrase 'parallel register architecture' does not provide sufficient teaching as to how the parallel nature of using/disposing registers as claimed can render the outset as being a 'parallel register architecture' because registers (even as disposed in parallel columns) cannot be themselves represent a whole computer architecture lacking sufficient teaching from the Specifications to corroborate such commonly-known concept;"[2]

Applicant has amended the claims to recite "CPU having parallel registers" in place of "parallel register architecture." As noted above, Applicant does not agree with the assertions made in the Office Action. However, Applicant has amended the specification in order to facilitate prosecution. Applicant does not concede that the language, which was objected to by the Examiner, is unclear as to context. Applicant respectfully reserves the right to reintroduce all original language.

35 USC §101 Rejection of the Claims

Claims 1-23 were rejected under 35 USC § 101 as being directed to non-statutory subject matter.

Discussion of Claim 1

The Office Action states:

> The whole operation is based on '**if** said register spill instructions can be associated' in the determination step, as such, the IF condition and its implication do not reasonably convey the existence of any alternate action other that the IF-dependent *rewriting* action as recited.[3]

[2] Office Action Page 3, Number 4
[3] Office Action Page 4, Number 6 (Emphasis in original.)

Applicant has amended claim 1 to recite, "determining **that** register spill instructions in spill code generated by a register allocator can be associated with each other." (Emphasis does not appear in the claim 1.)

Discussion of Claims 9, 16, and 20

Applicant has amended claims 9, 16, and 20 in a manner similar to that noted in the discussion of claim 1.

Discussion of Claims 2-8, 10-15, 17-19, and 21-23

Claims 2-8, 10-15, 17-19, and 21-23 each depend, directly or indirectly, on one of claims 1, 9, 16, or 20. As such, they include the features recited therein.

35 USC §112 Rejection of the Claims

Claims 1-23 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Discussion of Claims 1, 9, 16, and 20

The Office Action asserts that "there is no sufficient support in the claim as to clarify or render more explicit the meaning of 'can be associated', i.e. a mutual correspondence set forth by the elements recited as 'register spills instructions' and the act recited as 'be associated', when the context required for associating act entails at least 2 entities joined by an associating link."[4] Applicant has amended the claims to recite "associated with each other." Applicant submits that this amendment provides any needed clarity.

Discussion of Claims 7, 8, 14, 15, 18, 19, 22 and 23

The Office Action also rejected claims 7, 8, 14, 15, 18, 19, 22 and 23 as reciting "said memory stack" without antecedent basis. Applicant has amended claims 7, 8, 14, 15, 18, 19, 22 and 23 accordingly.

[4] Office Action Page 6, Number 8

35 USC §103 Rejection of the Claims

Claims 1-23 were rejected under 35 USC § 103(a) as being unpatentable over Kolson et al. ('A Method for Register Allocation Loops in Multiple Register File Architectures, Proceedings of IPPP's 96, 1996, pp. 28-33; hereinafter referred to as Kolson) in view of Kahle et al. (U.S. 5,867,684; hereinafter referred to as Kahle).

Discussion of Claim 1

Claim 1 has been amended to recite: "determining that register spill instructions in spill code generated by a register allocator can be associated with each other." In discussing claim 1 (before the current amendment), the Office Action construed claim 1's "determining whether register spill instructions... can be associated..." to mean that "the instructions are determined as to whether they can be reused or reloaded."[5] As such, the Office Action points to portions of Kolson that allegedly teach instructions that can be reused or reloaded.[6] Applicant submits that the current amendments clarify claim 1 and render the Office Action's discussion moot. Given the amendments to claim 1, Applicant submits that Kolson and Kahle, alone or in combination, do not teach or suggest claim 1's "determining that register spill instructions in spill code generated by a register allocator can be associated with each other."

Claim 1 also recites, "based on the determining, rewriting said register spill instructions as a parallel register spill instruction." In asserting that Kolson teaches this claim feature, the Office Action points to Kolson's Fig 4 and states "must be loaded from memory teaching or suggesting this claim feature."[7] Applicant presumes that the Office Action means that Kolson's variable being loaded from memory (or written from memory to a register) teaches or suggests the above-cited feature of claim 1. However, Applicant submits that writing a variable to a register does not teach or suggest rewriting multiple spill instructions into a single parallel spill instruction. Interestingly, the Office Action goes on to admit that Kolson *does not* "disclose rewriting spill instructions as a parallel register spill instruction."[8] Applicant agrees. The Office Action attempts to assert that Kahle provides what Kolson is lacking. In particular, the Office Action states:

[5] Office Action at page 6, Number 8, second-to-last sentence
[6] Office Action at page 7, Number 11
[7] Office Action Page 7, Number 11, second paragraph
[8] Office Action Page 7, Number 11, fourth paragraph

> "based on the structure of multiple banks of registers for concurrent operations in Kolson, it would have been obvious ... to apply a parallel register architecture instruction by Kahle to support the extended register banks as purported by Kolson for rewriting spill instructions as a parallel register instruction or loading spill instructions into said parallel register in parallel."[9]

However, Applicant submits that simply having the parallel instructions of Kahle does not teach or suggest claim 1's "based on the determining, **rewriting** said register spill instructions as a parallel register spill instruction." (Emphasis added.) Therefore, Applicant submits that the combination of Kolson and Kahle does not teach or suggest the above-cited feature of claim 1.

Claim 1 also recites:

> "based on said rewritten parallel register spill instruction, configuring storage of associated register spills in memory in such a manner that said register spills can be loaded back into said registers in parallel."

In asserting that Kolson teaches this claim feature, the Office Action points to Kolson's Fig 4 and states, "the update of register for runtime computation when variable [sic] are live and fetched from a memory discloses – by virtue of implicit teaching – a *load* back – see *must be loaded back from memory.*"[10] Later, the Office Action contradicts this by admitting that Kolson *does not* disclose "configuring memory spills by loading these into said parallel register in parallel."[11] Applicant agrees. Furthermore, Applicant submits that simply writing a variable to memory does not teach or suggest claim 1's "configuring storage of associated register spills in memory in such a manner that said register spills can be loaded back into said registers in parallel." As such, Applicant submits that the combination of Kolson and Kahle does not teach or suggest the cited claim feature.

Discussion of Claims 9, 16, and 20

Claims 9, 16, and 20 each include features similar to those noted in the discussion of claim 1. For at least those reasons, Applicant submits that the combination of Kolson and Kahle does not teach or suggest each and every element of claims 9, 16, or 20.

[9] Office Action Page 8, first paragraph
[10] Office Action Page 7, Number 11, third paragraph
[11] Office Action Page 7, Number 11, fourth paragraph

Discussion of Claims 2-8, 10-15, 17-19, and 21-23

Claims 2-8, 10-15, 17-19, and 21-23 each depend, directly or indirectly, on one of claims 1, 9, 16, or 20. For at least the reasons noted above, Applicant submits that the combination of Kolson and Kahle does not teach or suggest each and every element of claims 2-8, 10-15, 17-19, or 21-23.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (281-758-0025) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-3998

Respectfully submitted,

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